WHAT IS CLAIMED IS:

1. An apparatus for adjusting a sampling phase of a digital display, comprising:

a phase locked loop (PLL) circuit unit for converting a frequency of a sampling clock signal and outputting a converted frequency, the sampling clock signal for converting an analog video signal into digital format;

an analog to digital converter (ADC) for converting an incoming analog video signal into digital format using the sampling clock signal input from the PLL circuit unit to output a converted video signal;

a detection unit for detecting in a predetermined region a maximum phase shift of the converted video signal; and

a control unit for controlling the PLL circuit unit so that the sampling phase can be adjusted in accordance with the maximum phase shift detected by the detection unit.

2. The apparatus of claim 1, wherein the detection unit detects a number of phase shifts exceeding a predetermined reference level within the predetermined region, and when determining the number of phase shifts to be equal to, or greater than a predetermined value, detecting the maximum phase shift in the predetermined region.

3. The apparatus of claim 1, wherein the detection unit comprises:

a comparator that detects whether the converted video signal is varied to, or above a predetermined reference level based on the comparison between the converted video signal from the ADC and the reference level;

a counter that detects the maximum phase shift by counting an output signal from the comparator; and

a reference setting unit that inputs the predetermined reference level to the comparator for the comparison with the converted video signal.

4. The apparatus of claim 1, wherein the control unit, determining based on a signal output from the detection unit that the number of phase shifts exceeding the predetermined reference level is below the predetermined value, controls the detection unit to detect the maximum phase shift in another detection region.

5. The apparatus of claim 1, wherein the detection unit adjusts the sampling phase by computing one of 50% and 75% phases of entire checking region with respect to the maximum phase shift in accordance with a characteristic of the converted video signal.

6. A method for adjusting a sampling phase of a digital display, comprising the steps of:

a) converting an incoming video signal in a predetermined region into a digital format to output a converted video signal, and analyzing the converted signal;

b) determining whether a phase shift in the converted video signal analyzed in step a) varies at or above a predetermined level, and occurs more frequently than a predetermined value;

c) if the phase shift is determined to have occurred more frequently than the predetermined value, detecting a maximum phase shift of the predetermined region; and

d) adjusting the sampling phase in accordance with the maximum phase shift detected in step c).

7. The method of claim 6, wherein, if the phase shift exceeding the predetermined reference level is determined to have occurred less frequently than the predetermined value, changing a phase shift detection region, and returning to the step a).

8. The method of claim 6, wherein, after completion of the automatic sampling clock within the predetermined region, the step c) detects a maximum phase shift of the input signal while moving phase of pixel.

9. The method of claim 6, wherein the step d) adjusts the sampling phase by computing one of 50% and 75% phases of entire checking region with respect to the maximum phase shift in accordance with a characteristic of the converted video signal.